

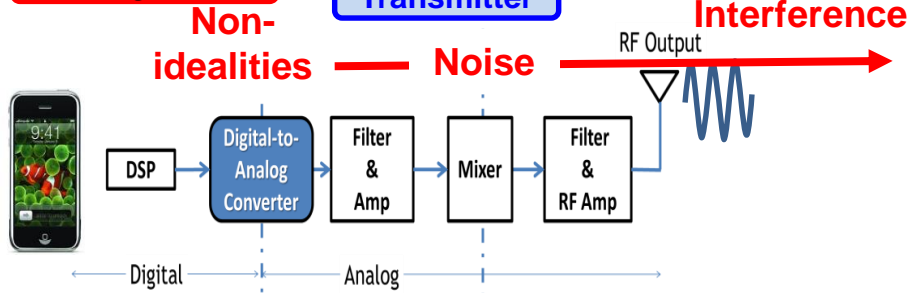
Linearity Improvement Algorithm for Current-Steering DAC Based on 3-Stage Sorting of Half-Unary Current Sources

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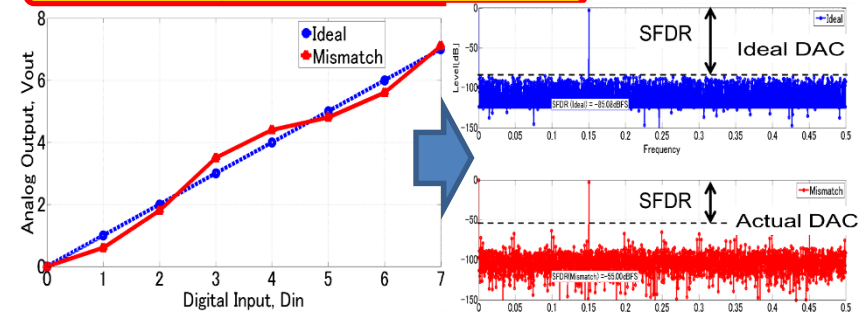
Background



Objective

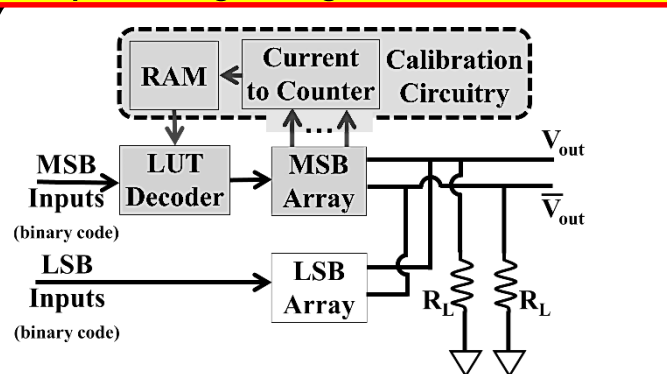
➔ Reduction errors due to circuit non-idealities!!

Static & Dynamic Performance



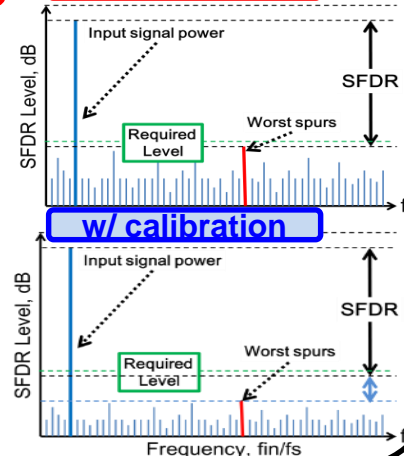
Effects ➔ Non-linearity & SFDR degradation !!

Proposed digital algorithm + calibration

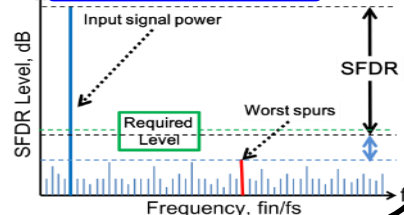


Current source sorting, rearranging
➔ Effectively reduced static error

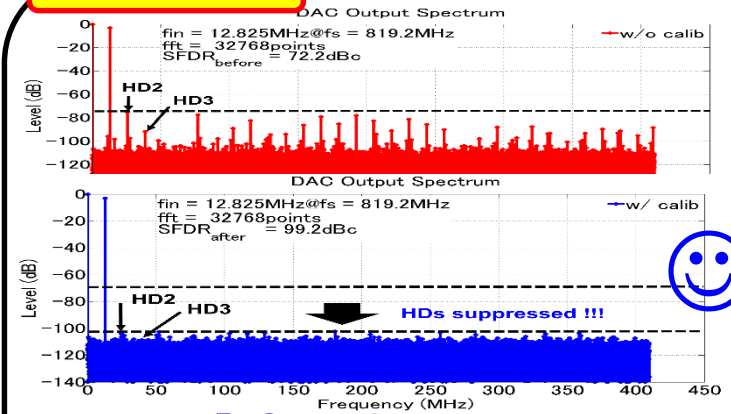
w/o calibration



w/ calibration



Achievement



Result ➔ SFDR improvement!!
➔ HD2 & HD3 suppressed!!